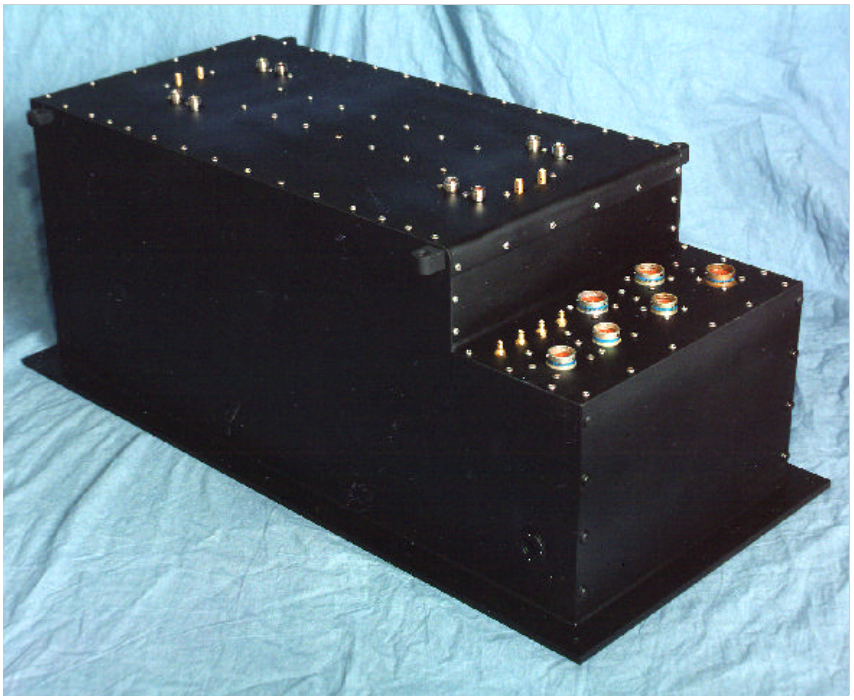
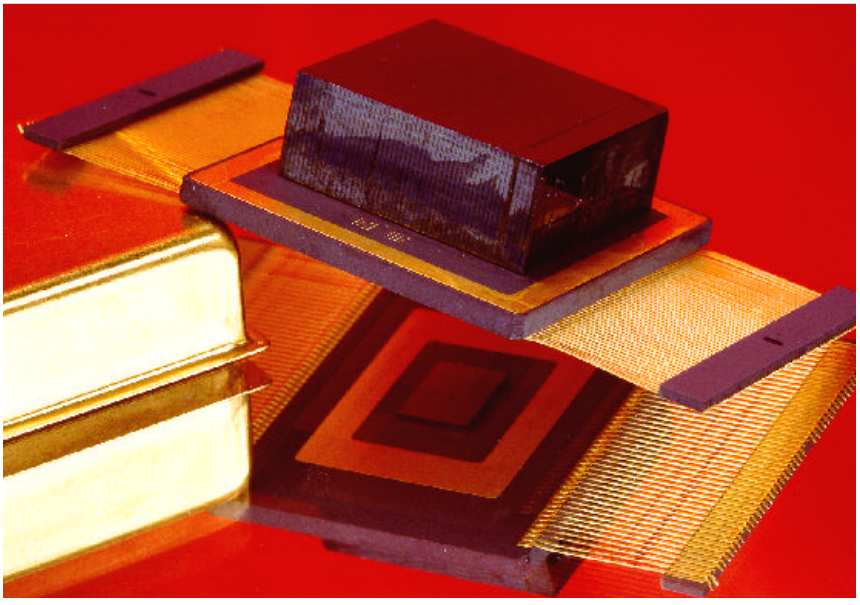
LOCKHEED MARTIN

Storage Unit LMSU-214G



Features

- Up to 214 Gbits at end-of-life (total of 280 Gbit including EDAC and redundancy)
  - 856 Gbit systems will be available when using 64 Mbit DRAMs
- Uses 16 Mbit IBM DRAMs
  - Assembled in 40 DRAM Irvine Sensors Corp (ISC) cube
  - >30 KRAD total dose
  - Latch-up immune
- 4 Gbaud I/O
  - 2 input and 2 output 1 Gbaud Fiber Optic Interface
  - Optional wire I/O available
- Control provided by redundant MIL-STD-1750A processors
  - MIL-STD-1553 control interface
- 80 pounds
- 12.25 ”x 26 ”baseplate x 10 ”height
- Radiation or cold plate cooling
- >.99 reliability for 5 years with no single point failures
- System bit error rate < 1E-14
- Power (28 VDC)
  - 110 W Simultaneous Read/Write (90 W for optional wire I/O)
  - 75 W Write or Read (65 W for optional wire I/O)
  - 40 W Data Retention
  - 15 W Standby
- System readily modified to support unique I/O and command interfaces



640Mb DRAM Cube Technology

Description

Lockheed Martin Federal Systems in Manassas, VA, offers a high density storage unit for use as a data buffer on satellite systems. A fully populated LMSU-214G contains up to 214 Gbit of usable memory at the end of a five-year mission. A pluggable subassembly design allows us to tailor the system to meet your specific data I/O requirements (up to 4 Gbaud per sec) and to satisfy your specific command interface and protocol.

The LMSU-214G is a high reliability system based on a memory module developed and qualified by Lockheed Martin Federal Systems. The LMSU-214G contains memory cubes manufactured by Irvine Sensors Corporation. Each cube has 40 fully functional IBM 16 Mbit Dynamic Random Access Memory (DRAM) devices.

Mounted on a ceramic substrate with a custom-designed radiation

hardened control ASIC, the memory cube is hermetically sealed and screened to class K specifications.

The system contains seven memory subassemblies, each of which is capable of being populated with 60 memory modules, or a total of 40 Gbits of memory.

The LMSU-214G is composed of two 107 Gbit (end-of-life) memory arrays sharing dual redundant controllers and power subsystems. Each memory array contains separate dual redundant fiber optic data interfaces. The system has no single point failures and contains fully redundant non-memory components.

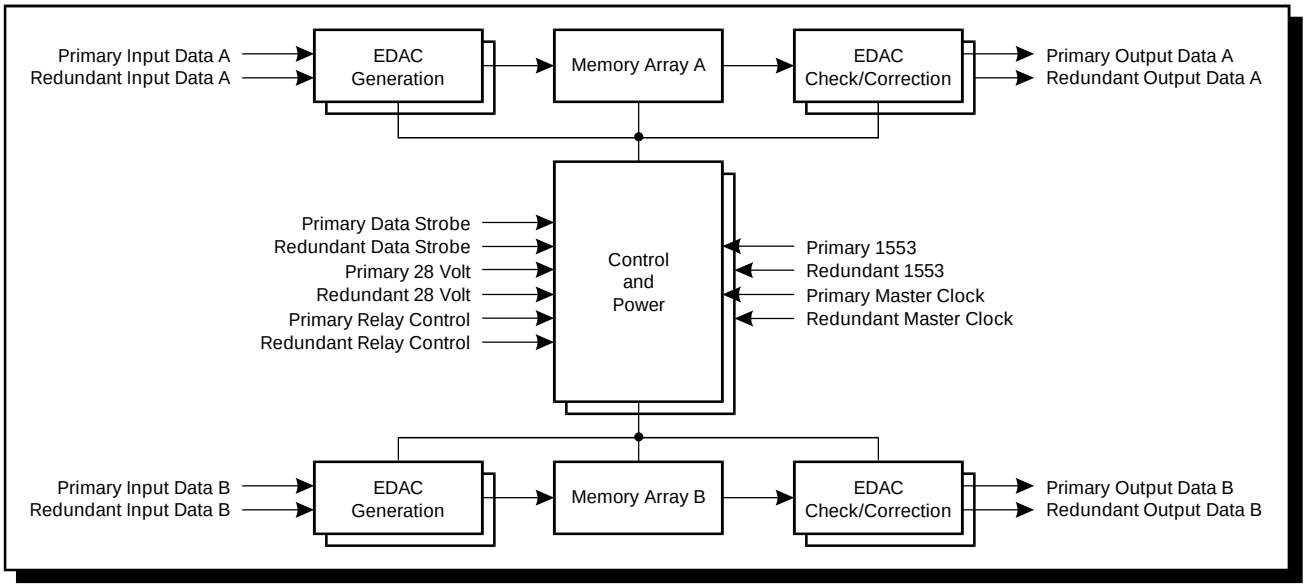
Redundant memory is provided within the memory array to ensure that a full 214 Gbits of storage is available for data storage at the end of a five-year mission with a reliability of .99. A Functional Block Diagram of the LMSU-214G is shown.

System control is performed by two redundant controller subassemblies, each containing a MIL-STD-1750A processor and dual redundant MIL-STD-1553 control interfaces. The operational and diagnostics software is stored in Electrically Erasable Programmable Read Only Memory (EEPROM) to allow ground reprogrammability. The memory data map is stored in Static Random Access Memory (SRAM). The interface command protocols can be readily modified to meet your specific requirements.

Redundant input and output data interfaces to the two memory arrays are provided on the four (identical) I/O subassemblies. A powerful symbol level Error Detection and Correction (EDAC) code, along with data scrubbing functions, are included on these subassemblies. The modular, plugable design of the LMSU-214G allows Lockheed Martin Federal Systems to readily tailor the I/O interface to meet your specific needs.

Power and power control functions are both fully redundant with sufficient margin to meet the LMSU-214G power needs well beyond the five-year system design life.

Lockheed Martin Federal Systems is currently accepting orders for the LMSU-214G and will tailor the system to address your specific data memory, data I/O, and command requirements.



Functional Block Diagram

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